[0056] A layer of conductor **218** is deposited, preferably by sputtering. A conductor mask is then provided, followed by etching, for example by wet or plasma etch, to isolate various conductor regions from one another. For example, the conductor for the gate contact (not shown) is isolated from the conductor **218** for the source/body/Schottky-rectifying contacts in this step. The conductor **218** in this specific example is an aluminum alloy, either by itself or over a material such as titanium tungsten, or a material such as platinum silicide that has been formed in the contacts, as it provides a Schottky rectifying contact at the bottom of trench **219***b*, while providing an ohmic contact at source/body regions **212**, **204**. The resulting structure is illustrated in **FIG. 6F**.

[0057] Of course, myriad variations on the above theme are possible. As one example, while the source regions **212** are provided in the above example prior to trench formation, it is also common in the trench MOSFET art to provide the source regions after formation of the trench gate structure. As another example, although oxide regions **216** are used above to isolate the polysilicon regions **211** from conductor **218**, BPSG is also commonly used for this purpose.

[0058] As noted above, the device design of the present invention can be implemented in connection with an essentially infinite variety of layouts in which DMOS transistors and Schottky diodes are integrated on the same silicon substrate. One particularly preferred layout is illustrated in **FIG. 8** and is referred to herein as an "unpacked octagonal geometry". This design includes alternating rows of relatively large and small octagonal cells.

[0059] Numerous variations of the unpacked octagonal geometry design are possible. For example, in **FIG. 8**, the Schottky cells are illustrated in connection with the rows of relatively small cells, but the Schottky cells could also be provided in connection with the rows of relatively large cells. In addition, although octagonal cells are illustrated in connection with the relatively small cell rows in **FIG. 8**, it is noted that the small cells could also be, for example, square cells as illustrated in **FIG. 10**.

[0060] One parameter by which the merged devices of the present invention can be characterized is the ratio of source perimeter to Schottky diode conducting area. As can be seen from FIGS. **9**A-**9**D, this ratio can be modified in various ways. For example, as can be seen from the design illustrated in **FIG. 9**D, the source perimeter for each of the large MOSFET mesas (four illustrated) is equal to (2×s1) +(2×s3)+(4×s2). The source perimeter for the small MOSFET mesas of **FIG. 10** is approximately 8×s2. The area occupied by the Schottky diode (one illustrated and designated with an "S") in **FIG. 10** is approximately (s2×s2). The unpacked octagon geometry illustrated allows the ratio of s2 to s1 as well as the ratio of s3 to s1 to be modified, within limits, which in turn allows great flexibility in dictating the ratio of source perimeter to the Schottky diode area.

[0061] For example, a magnified view of five cells from the structure of **FIG. 8** is illustrated in **FIG. 9A**. Each of these cells is a regular octagon. In **FIG. 9**B, however, the top, bottom, left and right sides (which correspond to lengths s1 and s3) are made significantly smaller than the diagonal sides (which correspond to length s2). As can be seen by comparing **FIG. 9A** with **FIG. 9**B, this acts to decrease the ratio of the source perimeter to Schottky diode area of the device of **FIG. 9**B, relative to the device of **FIG. 9A**.

[0062] On the other hand, the top, bottom, left and right sides (which correspond to lengths s1 and s3) can also be significantly larger than the diagonal sides (which correspond to length s2) as illustrated in **FIG. 9C**. This acts to increase the ratio of the source perimeter to Schottky diode area of the device of **FIG. 9**C, relative to the device of **FIG. 9A**.

[0063] In other embodiments, it may be desirable to increase the size of only the top and bottom sides as is shown in **FIG. 9D**. Of course, the size of the left and right sides could also be increased in a similar fashion.

[0064] Although various embodiments are specifically illustrated and described herein, it will be appreciated that modifications and variations of the present invention are covered by the above teachings and are within the purview of the appended claims without departing from the spirit and intended scope of the invention. For example, the method of the present invention may be used to form a structure in which the conductivities of the various semiconductor regions are reversed from those described herein.

1. A merged device comprising:

a plurality of MOSFET cells that comprise: (a) a source region of first conductivity type formed within an upper portion of a semiconductor region, (b) a body region of second conductivity type formed within a middle portion of said semiconductor region, (c) a drain region of first conductivity type formed within a lower portion of said semiconductor region, and (d) a gate region provided adjacent said source region, said body region, and said drain region; and

a plurality of Schottky diode cells disposed within a trench network, which comprise a conductor portion in Schottky rectifying contact with said lower portion of said semiconductor region;

wherein at least one gate region of said plurality of MOSFET cells is positioned along a sidewall of said trench network adjacent at least one Schottky diode cell.

2. The device of claim 1, wherein said gate region comprises a doped polysilicon region adjacent a silicon dioxide region.

3. The device of claim 1, wherein said first conductivity type is n-type conductivity and said second conductivity type is p-type conductivity.

4. The device of claim 1, wherein said semiconductor region is a silicon region.

5. The device of claim 4, wherein said semiconductor region is an epitaxial silicon region.

6. The device of claim 4, wherein said conductor comprises one or more of titanium tungsten, platinum silicide, aluminum and aluminum alloy.

7. The device of claim 3, further comprising a heavily doped contact region for contact to the body region.

8. The device of claim 3, further comprising a p-type region that is below the Schottky diode and contacts the perimeter of the Schottky diode.

9. The device of claim 1, wherein at least one of said MOSFET cells is octagonal in shape.

10. A merged device comprising:

a semiconductor substrate of first conductivity type;

a semiconductor epitaxial layer disposed over said substrate;